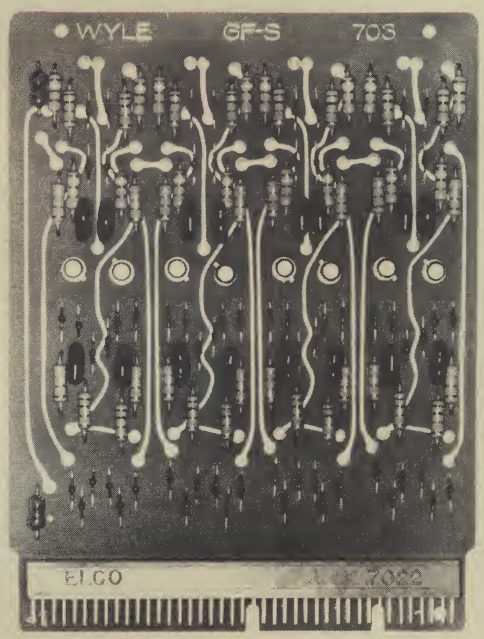
WYLE LABORATORIES PRODUCTS DIVISION



SILICON LOGIC MODULES

QUALITY, RELIABILITY & USABILITY AT LOWEST COST

This brochure introduces a new generation of silicon logic modules, modules which take advantage of the most recent developments in silicon components, circuit design, and manufacturing techniques.

The basic objective in the design of these modules was genuine usability. To achieve that objective, this line of modules offers the *reliability, economy,* and attention to details that constitute *integrity of design.*

MATERIAL & FABRICATION

The base material of the logic cards is 1/16 inch thick, flame resistant, glass impregnated epoxy. The conducting material is 2 oz. copper. Minimum conductor width and line spacing is a full .040 inches. Separate eyelets are used to connect etched patterns on the two sides of the board; no component leads are used for this purpose. Spray etching and wave soldering provide consistently uniform fabrication and eliminate the possibility of poor solder joints or irregular etching.

COMPONENTS

All components are derated from the manufacturer's specifications and the highest quality components are used throughout. All resistors are of the precision carbon film type featuring a low temperature coefficient which is consistent for all resistance values. Diodes are planar epitaxial with a whiskerless, rugged, micro-miniature double glass seal type construction. To increase end of life ratings, all transistors are operated well below the manufacturer's ratings of voltage, current and junction temperature. Gain-temperature characteristics are chosen to insure reliable, full specification operation over the range of —20°C to +70°C.

CIRCUITS

A complete selection of circuit types is available to implement virtually any type of system, and circuits are grouped on each card in the most useful logical configuration. The basic circuit is DTL NAND with clamped, saturated output. All inputs are diode coupled and isolated. All outputs are saturated transistors for logic zero and diode clamped collectors for logic one. All circuits have nodes brought to the connector, enabling the use of gate expanders, etc. Flip-flop modules of both AC coupled (using trailing edge triggering) and DC coupled types are included, as are gates, amplifiers, decoders, power drivers, oscillators, one-shots, and multivibrators. Distinction between AC (JK type) inputs and DC (RS type) inputs is solely for the case where inputs are from other than Wyle standard logic. When inputs are from other Wyle silicon logic modules, only the specified number of *unit loads* need be considered.

Extremely simple loading rules, based on a "unit load" system, are the only specification for interconnection of modules. As an example, a circuit with an output rated at 6 unit loads will drive *any* parallel combination of circuits whose input loads total six. This simple system allows even the novice designer to lay out complex logic systems with complete confidence.

A 41-pin connector allows maximum access to all important circuits, and free use of both external gate expanders and gate expanders on the modules themselves.

Test points are provided on all flip-flops, oscillators, multivibrators, one-shots, clock amplifiers, and Schmitt triggers. These are staked terminals for use with clip-on probes, rather than tip-jacks.

NOISE REJECTION

A most serious consideration, when assembling modules to form systems, is the control of noise. Noise signals generated by switches, indicators, electro-mechanical devices, and even other logic elements can be coupled into the inputs or outputs of a given logic element and cause spurious triggering, and since this type of malfunction is inherently transient and erratic in nature, it is particularly difficult to troubleshoot. Prevention of spurious triggering by building noise rejection capability into the circuits themselves is the surest and most straightforward approach to minimizing system noise problems.

Noise can be introduced into a system by any one of three routes: the input, the output or the power supply. Power supply noise is rejected by decoupling capacitors mounted on each logic module. Since the basic circuit of all systems is the flip-flop, it is used as the example in the following paragraphs which describe the noise rejection capability provided in Wyle silicon logic modules.

INPUT NOISE

A typical flip-flop input circuit and a typical driving source are shown in Figure 1. To begin with, it is difficult to generate a noise

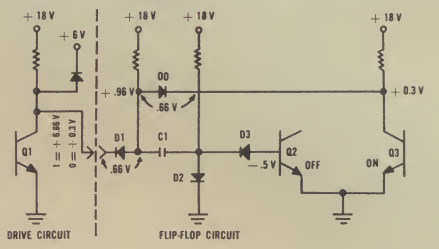


Fig. 1. Typical Flip-Flop input Circuit—Q2 off

pulse at the flip-flop input due to the low impedance of the driving circuit. If the driving circuit is at the logic zero level, the noise pulse must be generated across the impedance to ground, (typically less than 30 ohms) of a turned on transistor. If the output of the source circuit is at the logical one level, the noise pulse must be generated across the impedance to +6 volts (typically less than 50 ohms) of a turned on diode.

The circuit voltages shown in Figure 1 represent the case where Q2 is turned off. In this case, negative going transitions of the input voltage only tend to reinforce the existing conditions. Positive going transitions are decoupled by D3 and by D1. Furthermore, due to the clamping action of diode D0, D1 remains cut off for all voltage excursions, either positive or negative going, which are more positive than +0.3 volts.

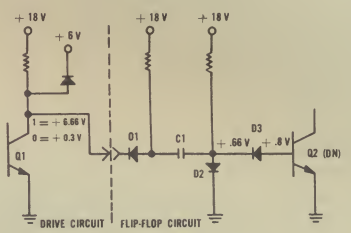


Fig. 2. Typical Flip-Flop input circuit—Q2 on

Figure 2 is the same circuit as Figure 1, but the voltages represent the case where transistor Q2 is turned on. Positive going transitions of the input voltage are decoupled by D3 and D1, as in the case with Q2 off. Furthermore, they are of no concern since they only tend to reinforce the existing conditions. Negative going transitions however, tend to turn Q2 off, reversing the state of the flip-flop: In this case, assume that a base voltage of —0.1 volts is sufficient to just turn off Q2. With a drop across the diode (VF) of 0.66 volts, this means the cathode of D3 must drop to —0.76 volts. Since this point is originally at +0.66 volts, due to the forward bias of D2, this requires a negative swing of +.66 —(—.76) = 1.42 volts. Note that this is a worst case and assumes C1 is a direct short, or in other words, that the noise pulse has an infinitely fast negative going transition.

OUTPUT NOISE

Noise is most frequently introduced into circuits via the output leads. Large numbers of output leads from registers, counters, etc., are often terminated in one connector or routed in bundles to visual displays, controls, or other logic sub-systems. Pulses on one of these wires can easily couple into an adjacent lead. To prevent spurious triggering, the Wyle silicon flip-flop modules use the circuit shown in Figure 3.

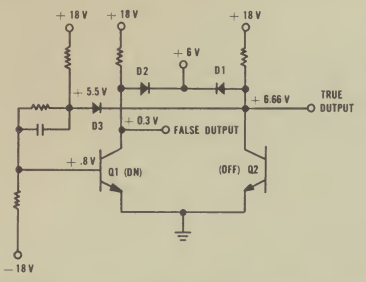


Fig. 3. Flip-Flop output circuit

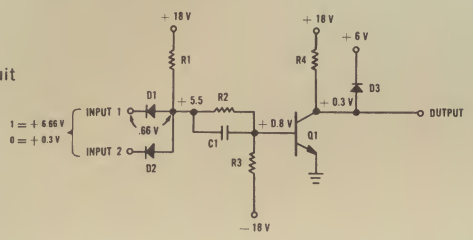
The voltages shown in Figure 3 represent the case when the true output is at +6.66 volts (Q1-on; Q2-off). In this case, positive noise signals generated at the output must be generated across the low impedance of a "turned on" diode (D1) and serve only to further reverse

bias D3. With D3 reverse biased, no noise pulses can be coupled to the base of Q1. A negative pulse must pull the cathode of D3 to +4.84 volts (+5.5 — Vf) before D3 conducts. Since the output is at +6.66 volts, this requires a drop of —1.82 volts.

When the true output is at the logical zero level, diode D3 is conducting and the states of the transistors are reversed (Q1-off; Q2-on). Noise signals for this case must be generated across the low impedance of the turned on transistor Q2. In this state, a negative pulse only turns Q1 further off and does not affect the state of the circuit. A positive pulse must raise the anode of D3 to a point sufficiently positive to raise the base voltage of Q1 to +.8 volts. This requires an anode voltage of approximately +4.5 volts. The output is nominally at +.3 volts and must rise to (+4.5 — Vf), or about +3.84 volts, requiring a total rise of about +3.5 volts.

The previous discussion is limited to the noise rejection characteristics of flip-flop circuits. An example of the characteristics of the other basic circuit, the typical NAND gate is shown in Figure 4.

Fig. 4. Typical Nand circuit



The power supply voltages and ratios of resistances have been chosen to insure noise rejection. Figure 4 shows typical voltages in the circuit when both inputs are at the logical one level and the output at the logical zero level. Positive noise signals are blocked by diodes D1 and D2 and negative noise must drop to (5.5 — Vf) volts to forward bias either diode. The required voltage drop to affect the circuit is therefore —1.82 volts minimum.

If either or both inputs are at logical zero, then negative noise will only reinforce the existing condition. Like the flip-flop circuit, the ratio of R1 and R2 has been selected so that a positive swing of approximately +3.5 volts is required in order to affect Q1.

GENERAL SPECIFICATIONS

Logic Levels:	
Logical "One"	+6.6±0.3 volts
Logical "Zero"	+0.25±0.25 volts
Operating Temperature Range:	—20°C to +70°C
Operating Frequency:	
Logical circuits	DC to 1.5 Mc
Display and Relay Drivers	DC to 1 Kc
Power Supply Voltages:	+18V, +6V, —18V
Fan In:*	10
Fan Out:	See individual specifications
Physical Dimensions:	
Width	4½ inches
Length	6 inches
Mounting	9/16 inches minimum center-to-center
Connectors:	41 pin Elco Varicon
Keying:	2 slots for individual keying of all types.

***NOTE:** Fan In is defined as the maximum number of parallel lines (AND gates) which can be connected to one input without degrading the waveform sufficiently to impair operation.

The basic line is composed of 19 card types which include all the logic, interface modules, and accessories necessary for most systems. These card types are:

BF-S — 4 binary flip-flops. Normally functions as scale of 16 counter; easily converted to scale of 10 by two external straps. Diodes are provided for individual pre-setting of each flip-flop.

CF-S — Six control flip-flops. RS types for buffer storage and control. Additional master reset line simultaneously resets all six flip-flops.

GF-S — 4 general purpose flip-flops. Can be used as independent JK or RS flip-flops or externally strapped to perform various functions.

NG-S — NAND gates. Three—3 input gates, three—2 input gates, two—2 input gate expanders, two—1 input gate expanders. All nodes brought to connectors.

IAS — Ten inverting amplifiers, one—2 input gate expander, two—1 input gate expanders. Inverters are actually one input NAND circuits and all nodes are brought to connector.

GE-S — Gate expanders. Six—2 input, eight—1 input circuits, plus one inverter with node brought out.

PD-S — Ten inverting power drive circuits, each capable of switching loads up to 200 ma maximum at up to 50 volts maximum. Each input is a two term AND gate. One input of each gate is tied to one of two "inhibit" lines, each of which controls five circuits. Nodes are brought out to the connector from all circuits.

PA-S — Five inverting power driver circuits, each capable of switching loads up to 1 amp. at voltages up to 50 volts maximum. Each input is a five term AND gate which permits direct decoding of BCD inputs, with one input of each gate tied on an "inhibit" line which controls all circuits. All nodes are brought out to the connector. The drivers are actually power switches which complete the circuit from an external power supply, through the load to ground.

DM-S — Decimal conversion matrix. Normally arranged to convert two 1248 BCD digits to one-out-of-ten code. Can be externally strapped to convert four binary bits to one-out-of-sixteen, or one-out-of-ten for any four line code, such as excess—3, 1224, etc.

DD-S — BCD to Decimal decoder and driver. Converts 1248 BCD digit to one-out-of-ten code with an amplifier on each output line capable of handling 50 volts maximum, at 200 milliamps maximum, for driving visual displays, etc.

CD-2 — Four 2-input clock drivers, four 2-input NAND, one 2-input gate expander, one 1-input gate expander. The clock drivers allow signals to be distributed to large synchronous logic systems.

KO-S — Crystal controlled oscillator which provides both normal and inverted outputs, each via a gated buffer amplifier. The module also provides a 3-input gated clock driver circuit and three—2-input gate expanders.

MV-S — Two astable multivibrators. Both normal and inverted outputs are provided, all through buffer amplifiers. Frequency ranges are selected by connector wiring of capacitors mounted on the card. Potentiometers provide fine frequency adjustment of each range. The total frequency range is from 1 Mc to 100 cps and external capacitors can be used to obtain even lower frequencies

ST-S — Two Schmitt triggers and two AC amplifiers. All inputs and outputs are brought out to the connector. The Schmitt triggers can be adjusted to trigger on positive levels, negative levels, or zero crossing, and are provided with an adjustable hysteresis. The AC amplifier can be externally strapped to provide gains of X1, X10, or X100.

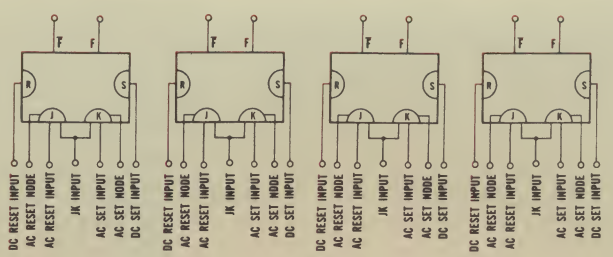
LI-S — Ten level shift amplifiers. These are universal circuits designed to accept inputs from either "positive true," "negative true," or hybrid positive-negative circuits and convert the signals to standard Wyle logic levels.

NI-S — Twelve neon indicators and drivers. Indicators are mounted at the end of the board opposite the connector. Useful for binary shift registers, counters, etc.

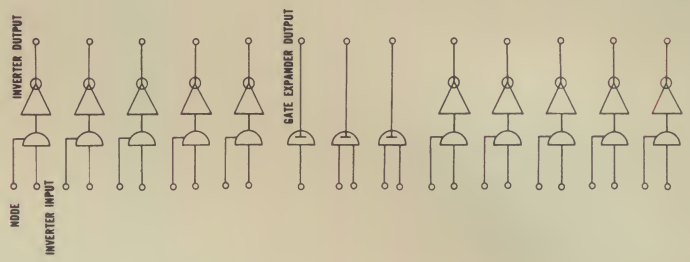
AG-S — AND gates. Three—3 input and three—2 input AND gates with two—2 input gate expanders and two—1 input gate expanders. All nodes are brought to the connector and each gate output is via non-inverting amplifiers for additional drive capability.

EC-S — Extender card. Consists of a board with a plug at one end and a receptacle at the other, connected by etched conductors. The board is inserted in a card file and a logic module can be inserted in the receptacle and is then accessible for testing while still connected to the system.

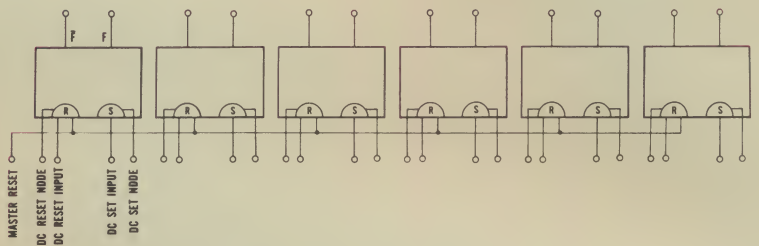
MODEL GF-S **PRICE: $75.00**
GENERAL PURPOSE FLIP-FLOP MODULE
(FOUR JKRS TYPE CIRCUITS)

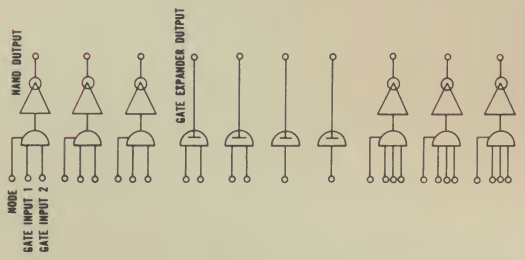


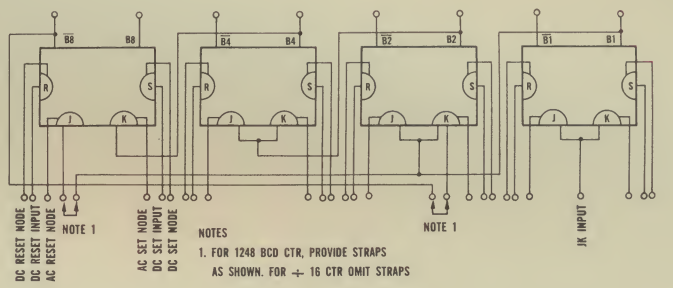
MODEL IA-S **PRICE: $50.00**
INVERTER AMPLIFIER MODULE



MODEL CF-S **PRICE: $70.00**
CONTROL FLIP-FLOP MODULE
(SIX SET-RESET TYPE CIRCUITS)



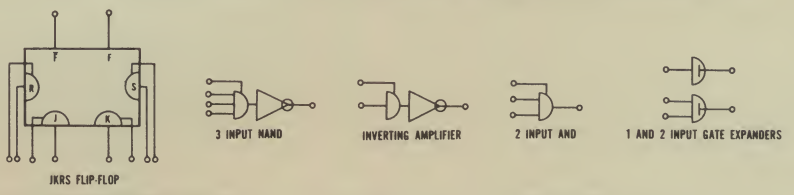




MODEL NG-S **PRICE: $45.00**
NAND GATE MODULE

MODEL BF-S **PRICE: $75.00**
BINARY FLIP-FLOP MODULE (SCALE OF 16 OR SCALE 10 COUNTER)

STANDARD LOGIC SYMBOLS



- *The quality of the most modern and advanced components*
- *The quality of modern production techniques*
- *The quality of the finest materials and design*
- *The reliability of silicon components*
- *The reliability of conservative specification*
- *The reliability of worst case design and thorough testing*
- *The usability of system oriented circuit design*
- *The usability of maximum access to all circuit components*
- *The usability of simplified loading rules*
- *All at prices approximately one-half to one-third less than competitive products*

WYLE LABORATORIES PRODUCTS DIVISION
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